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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Bruno GHYSELEN et al.	Confirmation No.: 7326
Patent No.: 7,018,910 B2	Application No.: 10/614,327
Patent Date: March 28, 2006	Filing Date: July 8, 2003
For: TRANSFER OF A THIN LAYER FROM A WAFER COMPRISING A BUFFER LAYER	Attorney Docket No.: 4717-7600

REQUEST FOR CERTIFICATE OF CORRECTION UNDER 37 C.F.R. § 1.322

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Patentees hereby respectfully request the issuance of a Certificate of Correction in connection with the above-identified patent. The correction is listed on the attached Form PTO-1050. The correction requested is as follows:

Column 12, line 31 (claim 6, line 3), after "substantially relaxed" delete "stale" and insert -- state --. Support for this change appears in original application claim 7.

The requested correction is for an error that appears to have been made by the Office. Therefore, no fee is believed to be due for this request. Should any fees be required, however, please charge such fees to Winston & Strawn LLP Deposit Account No. 50-1814. Please issue a Certificate of Correction in due course.

Respectfully submitted,

4/4/06
Date

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UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO.: 7,018,910 B2
DATED: March 28, 2006
INVENTORS: Ghyselen et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 12,
Line 31, after "substantially relaxed" delete "stale" and insert -- state --.

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such as finishing treatments like a heat treatment, to further strengthen the bonding interface with the receiving substrate **5**. Where a heat treatment, such as an annealing step is carried out. During annealing, defects, such as pinholes, can appear in the crystalline structure of the wafer. The annealing can be conducted prior to the removal of the strained layer **3** from the relaxed layer **4** so that the strained layer protects the relaxed layer **4**.

Optionally, after the splitting, the remaining portion of the matching layer **2** is removed from the strained layer, and the strained layer can be grown further, such as epitaxially, and can be oxidized. The oxidation can reduce or substantially prevent diffusion of germanium from the relaxed layer **4**. As explained in WO99/52145, the presence of SiO_2 can help protect against these defects during annealing. The further growth of the strained layer is preferably conducted to thicken this layer to repair damage thereto caused by the removal, such as by etching, of the remaining portion of the matching layer. The regrowing may be carried out to thicken the strained layer back to its original thickness, and in any embodiment the regrowing is conducted preferably to maintain the thickness of the strained layer at less that its critical thickness, beyond which the strain in the layer is relaxed and defects can appear in the crystalline structure.

In one embodiment, the thickened strained layer can be used as an active layer to take advantage of the increased electron mobility, instead of removing the strained layer.

Other embodiments of the invention employ other materials for the matching layer **2**, which may not include an SiGe lattice parameter matching layer **2**, and may include a matching layer **2** made from other types of type III-V materials or other materials capable of providing the desired lattice parameter in the film **3** to match that of relaxed layer **4**, including materials capable of straining the material of the epitaxially overgrown film **3**. These materials preferably include indium, gallium, arsenic and combinations thereof such as gallium arsenide.

The present invention can be used for transferring other materials, instead or in addition to a relaxed SiGe layer **4**, and may be used for transferring a layer of any type of semiconductor capable of being transferred according to the inventive method and to produce the inventive wafer Also, in each layer, including the semiconductor layers, other constituents may be added, such as carbon. The carbon may be added in a carbon concentration in the respective layer of less or substantially less than 50% by weight in one embodiment, about 50% in another embodiment, and more than 50% in another embodiment. A preferred carbon concentration is less than or about 5% by weight.

While illustrative embodiments of the invention are disclosed herein, it will be appreciated that numerous modifications and other embodiments may be devised by those skilled in the art. Therefore, it will be understood that the appended claims are intended to cover all such modifications and embodiments that come within the spirit and scope of the present invention.

What is claimed is:

1. A method of preparing a semiconductor wafer, comprising:

growing a first layer of a first material in a strained state on a matching substrate comprising a matching layer;

growing a second layer of a semiconductor second material, different from the first material, in a relaxed state on the first layer to form a boundary between the first and second layers and to form a composite structure which comprises the matching, first, and second layers, wherein the first and second layers each have substantially the same first lattice parameter;

creating a region of weakness in the matching substrate to facilitate splitting;

splitting the composite structure at the region of weakness into:

an unfinished wafer that includes the second layer, the first layer, and at least a remaining portion of the matching layer, and

a handle wafer:

removing the remaining portion of the matching layer from the first layer; and

removing the first layer from the second layer to produce a surface on the second layer that is substantially smooth and of substantially uniform thickness.

2. The method of claim **1**, wherein the matching layer has the lattice parameter where it contacts the first layer that is substantially the same as the first lattice parameter of the first layer.

3. The method of claim **1**, further comprising growing the matching layer on a handling substrate that has a second lattice parameter that is different from the first lattice parameter.

4. The method of claim **1**, wherein the matching layer includes a buffer layer and a relaxed surface layer.

5. The method of claim **4**, wherein the lattice parameter of the matching layer is graded between the first and second lattice parameters.

6. The method of claim **5**, wherein the region of weakness is created in a portion of the matching layer that is in a substantially relaxed stale. state

7. The method of claim **1**, further comprising associating a receiving substrate with the second layer of the composite structure prior to splitting.

8. The method of claim **7**, wherein the receiving substrate is bonded to the second layer.

9. The method of claim **7**, further comprising providing an insulator between the second layer and receiving substrate.

10. The method of claim **1**, wherein the region of weakness is created by implanting atomic species.

11. The method of claim **1**, wherein the region of weakness is created by adding a porous layer.

12. The method of claim **1**, wherein the first layer is strained to impart the first lattice parameter.

13. The method of claim **12**, wherein the lattice parameter of the first material when strained is different than the lattice parameter of the first material in a relaxed state.

14. The method of claim **1**, wherein the first layer is removed by etching.

15. The method of claim **14**, wherein the remaining portion of the matching layer is removed from the unfinished wafer by etching.

16. The method of claim **1**, wherein the boundary with the first layer removed is sufficiently smooth for growing a substantially uniform and substantially smooth device layer thereon of a semiconductor material that is different from that of the second layer and that has a lattice parameter that is adapted to match that of the second layer.

17. The method of claim **1**, wherein the first material is a semiconductor.

18. The method of claim **1**, further comprising growing a device layer on the surface.

19. The method of claim **1**, wherein the region of weakness is created at a depth from the second layer sufficient for substantially preventing damage to the second layer.